286 LX SERIES
USER'S MANUAL

286 LX Series System

(286 LX-A and 286 LX-M)

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STARTING UP THE SYSTEM

Power up the system and wait for the system to show up the system activity on the screen.

MEMORY TEST BYPASS

The system performs diagnostics of the system and displays the size of the memory being tested.

Note that you can bypass the memory test by pressing the <ECS> key. This option would be quite useful when the memory on the system is quite large. You should hit the <ESC> key when the message Press <ESC> Key to bypass MEMORY test appears on the screen.

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286 LX Series System

(286 LX-A and 286 LX-M)

INTRODUCTION

The mother board used for the 286 LX series is a fully IBM PC AT compatible baby board based on the VL82PCAT 5-chip IBM PC AT compatible chip set. The mother board is implemented in an IBM PC/XT compatible form factor, but mounting holes are provided for AT-chassis mounting. This mother board implementation provides jumpers to allow for all of the features of the VL82PCAT set to be evaluated. In this board, only 18 non-memory components (38 total components, including the TTL delay line) are required allowing for a minimum chip count implementation.

In this document, the following terms are VLSI-specific and require a more detailed explanation.

After that, the setup takes two different paths depending upon the CMOS being initialized or uninitialized.

CMOS Initialized

Under these conditions you would see the following messages :

Fixed disk drive C type:X(if installed else Not Installed.)

Fixed disk drive D type:X(if installed else Not Installed.)

Diskette drive A is 3 1/2"
Diskette drive B is :Double Sided (Other options as above)
Base Memory Size is :XXX KB
Expansion memory size is:XXXX KB

Are these options correct (Y/N)?

Note that the information about Dirive A indicates 3 1/2", as CMOS had been set earlier to reflect this status. If on the contrary, CMOS had been set for a 1.2 MB drive, the message in place of 3-1/2" it would be High Capacity.

If you feel that the information displayed above is right hit <Y> and the <ENTER> key to proceed to system boot with the new information.

CMOS Uninitialized

Disk Drive Type Definition

In this case you would have to enter the type of the fixed Drive C in response to the message:

.....WARNING.....

Entering the wrong disk drive TYPE causes improper operation of the disk.
If disk not installed press <RETURN> For disk TYPE details press <ESC>

Enter disk drive type (1-47)?

Note that the disk type details are only a key stroke away. Hit <ESC> key to find for yourself. You could always come back by hitting <ESC> again. Refer to Appendix B for drive details.

Once you have convinced yourself about the drive type enter the appropriate number and hit <ENTER>.

Note that pressing <ENTER> key alone indicates the absence of the Drive C.

CLOCK MODULATION

This feature automatically switches the processor clock speed from 12MHz down to 8MHz or 6MHz when an I/O operation is detected. This allows peripherals that have access time problems to function properly with a processor running at 12MHz.

System Board Features of the 286 LX-A and 286 LX-M Systems

- Supports up to 12MHz system operation (optional 10MHz system operation)
- Norton SI Benchmark rating of 15.3
- 0 wait state READ operation
- 1 wait state WRITE operation
- Clock modulation for 8/6MHz or 12/10MHz system operation with Turbo indicator
- Fully IBM PC AT compatible
- 4MB onboard DRAM, 100ns access time
- IBM PC/XT size form factor (AT mounting holes)
- 20mA, 200pF slot drive capability
- 8mA, 150pF DRAM drive capability
- 4-layer implementation for low-noise operation
- Minimum component count implementation

SUMMARY OF SET-UP

The Set-Up screen thus requires you to set
a). Date.
b). Time.
c). Hard Disk Type For Drive C (if present)
d). Hard Disk Type For Drive D (if present).

The Set-up precedure also automatically detects the following:

a) Type Of Display Card.
b) Size Of Real Memory.
c) Size Of Memory beyond 1 MB.
d) Presence of 360kb floppy drives.
e) Presence of a 80287.

Also, if a second Hard Disk drive is physically connected but the CMOS is not set for this Drive D, the SYSTEM informs you about the same and gives you a chance to configure the drive through SETUP

Having setup the CMOS, the SYSTEM runs through the diagnostics again, tests the memory, sets up the devices configured and proceeds to boot.

Note that the Set-up option is available even after a soft reset.

When does The SYSTEM Prompt You to Run Set-up?

The SYSTEM prompts you to run Set-up under the following conditions

a) CMOS options not set.
b) Display Configuration Mismatch
c) Memory Size mismatch.
d) Hard Disk Set-up error.
e) CMOS battery is low.
f) An additional hard disk presence is detected.

Errors Reported By SYSTEM

SYSTEM performs various diagnostic tests at the time the system is powered up. Whenever an error is encountered during these tests either you hear a few short beeps or see an error display on your monitor. If the error occurs before the display device is initialised the system reports the error by giving a number of short beeps.

If the error is FATAL the system halts after reporting the FATAL error. If the error is NON-FATAL the process continues after reporting the NON-FATAL error.

In the diagram, the VL82C100 replaces the bulk of the LSI peripherals used in the PC/AT, while the other components replace MSI and SSI components. In this diagram, the system shown is for 12MHz with zero wait state and 1MB of RAM (1 wait state for reads is an option available with the use of 120ns DRAMs). For various design reasons, certain peripheral functions were left outside of the VL82CPCAT chip set. These include the 146818 Real-Time Clock with its oscillator (14069) and the 8742 keyboard controller. Also left outside are some of the memory control circuitry.

Processor

The 286 LX baby board contains an 80286 processor running at 12MHz (slower speeds optional) with a processor clock cycle time of 83.3ns, and an average memory cycle time of 175ns (0 wait state on reads, 1 wait state on writes with a read/write ratio of 9:1). These memory cycle times are more than twice as fast as the memory cycle times of an 8Mhz IBM PC AT running with one wait state.

Math Coprocessor

A socket is provided for an optional 80287 math coprocessor. The coprocessor runs on a clock that is the same as the processor. For full speed operation, a 10MHz coprocessor is required.

Onboard RAM

The 286 LX-A contains space for 36 16-pin or 18-pin DRAMs that can contain either 64KB, 256KB or 1MB DRAMs.

The 286 LX-M contains space for 36 16-pin DRAMs that can contain either 64KB or 256KB DRAMs, and 4 30-pin module DRAMs that can contain 256KB or 1MB DRAMs.

When populated with a combination of 256KBs and/or 64KBs, the 286 LX can support memory maps of 512KB, 640KB, 1MB, 2MB or 4MB.

Onboard ROM

The 286 LX contains sockets for 2 BIOS EPROMs that can either be 27128s or 27256s. The access times for the EPROMs can be either 120ns with 1 wait state or 200ns when using 2 wait state accesses. ROM access cycles are either 3 or 4 processor cycles long.

USE OF 3 1/2" SUPPORT EFFECTIVELY

DOS 3.20 provides support for 3 1/2" drives. Earlier versions of DOS would require the use of DRIVER. SYS to provide the necessary support.

The 3 1/2" drive can be freely configured as drive A or Drive B with this BIOS. Thus it is possible to boot off directly from a 3 1/2" drive.

A few points would have to be kept in mind when you perform the Setup you define the drives correctly. Incorrect definition could make the drive unusable.

The table below describes the valid combinations on an AT.

CMOS Status	Physical Drive Status	Functional
1.2MB	1.2MB	YES
3 1/2"	3 1/2"	YES
Undefined	1.2MB	YES

DIAGNOSTICS

Diagnostics Menu

The Diagnostics memu as seen on the screen is shown in Fig. 1 of Appendix B.

Note the following in the Diagnostics Opening Menu:

a) The Guide Line in Reverse Video specifying the usage of the Cursor Keys, <ENTER> & <ESC> key.

b) The Configuration of the system in the "Devices Present" box.

c) The Real Time Clock ticking away at the right hand top corner of the screen.

d) Diagnostics Options Line - Hard Disk, Floppy, Keyboard, Video & Miscellanceous Diagnostics.

e) Hard Disk Diagnostics Options Window - detailing the various hard disk diagnostics that are available.

Table 1 Interrupt Controllers

Priority	Source	Destination
NMI	Parity Error	80286 NMI
0	Timer Channel 0	Master PIC, Int 0
1	Keyboard Controller	Master PIC, Int 1
2	Slave PIC	Master PIC, Int 2
3	Clock/Calendar	Slave PIC, Int 0
4	8-bit Slot, IRQ 9	Slave PIC, Int 1
5	16-bit slot, IRQ10	Slave PIC, Int 2
6	16-bit slot, IRQ11	Slave PIC, Int 3
7	16-bit slot, IRQ12	Slave PIC, Int 4
8	Math Coprocessor - Busy	Slave PIC, Int 5
9	16-bit slot, IRQ14	Slave PIC, Int 6
10	16-bit slot, IRQ15	Slave PIC, Int 7
11	8-bit slot, IRQ 3 (Serial Port)	Master PIC, Int 3
12	8-bit slot, IRQ 4 (Serial Port)	Master PIC, Int 4
13	8-bit slot, IRQ 5 (Printer Port)	Master PIC, Int 5
14	8-bit slot, IRQ 6 (Flex Disk Drive)	Master PIC, Int 6
15	8-bit slot, IRQ 7 (Printer Port)	Master PIC, Int 7

DMA Controllers

The VL2C100 contains 2 82C37A DMA Controllers that handle both 8-bit byte and 16-bit word transfers. These controller operate at 1/2 of the processor clock speed (processor running at 12MHz corresponds to DAM Controller running at 6MHz). Table 2 lists the usage of the DMA channels and the corresponding signals that drive them.

Table 2 DMA Channels

Slave DMA Channel #	Master DMA Channel #	Device
0	-	8-bit Slot, DRQ 0
1	-	8-bit Slot, DRQ 1
2	-	8-bit Slot, DRQ 2
3	-	8-bit Slot, DRQ 3
-	4	Slave DMA Controller input to Master DMA
-	5	16-bit Slot, DRQ 5
-	6	16-bit Slot, DRQ 6
-	7	16-bit Slot, DRQ 7

All the options under Hard Disk Diagnostics require more or less the following inputs:

a) Disk Drive
b) Drive Type
c) Interleave Factor
d) Bad TRack List
e) Start Cylinder
f) End Cylinder
g) Start Head
h) End Head

All the above input fields have a default value. Thus a user need not necessarily key-inall the inputs.

We shall discuss the inputs required & their meaning for Hard Disk Format Option. This discussion can however be expended for the rest of the Hard Disk Options.

Hard Disk Format Option - (Destructive Operation)

Figs 6 & 7 reflect the various screens the user goes through when this option is selected.

Note that in case of a single drive System the disk drive for the operation is assurmed to be drive D.

a) Drive Type Definition

The default value for the drive type is the SETUP value set during the CMOS setup.

However if the drive was not set during CMOS Setup, the user now has an option of setting the drive to be one among the 46 atandard Disk drive types.

Note that all the information about the drive unfolds when the disk dirve type is being chosen.

Ref. Fig.6 depicting the way the screen looks when this option is chosen.

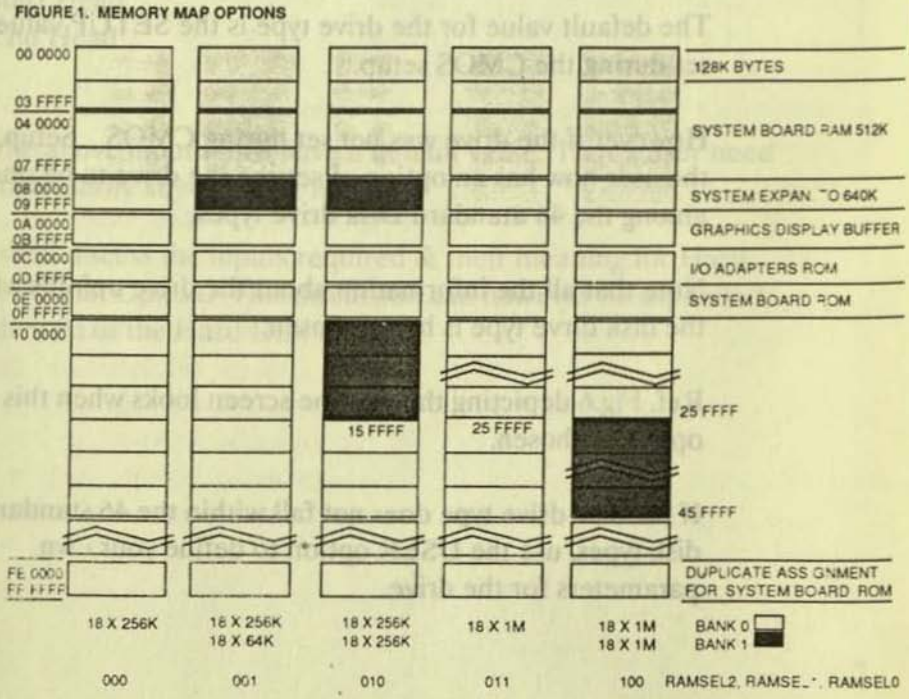
If the disk drive type does not fall within the 46 standard disk types, use the USER option to define your own parameters for the drive.

Memory Maps

The 286 LX supports 5 memory maps ranging from 512K to 4MB.

Any memory reference made to an address outside of the range will be directed toward the system expansion bus. The available maps for this card are shown in Figure 2.

Figure 2 Memory Map Options



THE MAIN BOARD CONNECTORS, JUMPERS AND SWITCHES

The main board connectors, jumpers and switches are used to configure your system.

The jumpers are used to configure a variety of options that are supported by the VL2CPCAT chip set. These jumpers are described in the following sections.

Connections to the 286 LX must be made through different types of connectors in different places. The description of the connectors are shown in the following sections. Note that the external battery that supplies the RTC should be between the range of 3.6 to 6VDC.

The Jumpers, Connectors and Switches in 286 LX-A

The location and function of each of these connectors, jumpers or switches are shown in Table 4.

g) Activity Screen

SYSTEM then proceeds to format the Hard Disk with th e specified parameters. While it is formatting SYSTEM displays the Operation in progress, the Cylinder & Head No. that is being formatted.

You could always hit <ESC> key to abort the format operation.

Auto Interleave Option - (destructive Operation)

This is the most powerful feature which enables you to get the peak performance out of your Hard Disk.

With this feature you need not speculate about the value of the Interleave Factor. SYSTEM is entrusted with the job of finding the optimum Interleave value by a trial & error method & formatting the Hard Disk with this value.

Discover the big advantage with this feature.

Media Analysis Option - (Destructive Operation)

Media analysis performs the following operations on the Hard Disk:

- Preformats the Hard Disk with specified parameters like Format Option.

- Analysis the surface of the Hard Disk for any errors & makes a note of them.

- Marks the Bad Patches.

This takes quite some time & for best results this test should run uninterrupted.

The parameters required for this are to be inputted in the same way like the Format Option.

J19 and J20 (Power Connectors)

The pin assignments for the power connectors J19 and J20 are as follows:

J19:

Pin	Assignment	Color
1	Power Good	orange
2	+5v	red
3	+12V	yellow
4	-12V	blue
5	GND	black
6	GND	black

J20:

Pin	Assignment	Color
1	GND	black
2	GND	black
3	-5V	white
4	+5V	red
5	+5V	red
6	+5V	red

J22 (External Battery Connector)

The pin assignments are as follows:

Pin	Assignment
1	V+
2	NC
3	GND
4	GND

As in the case of hard disk the list below gives the effect of each of the diskette tests:

a) Diskette Format - Destructive.
b) Speed Test - Non-destructive.
c) Random R/W Test - Destructive
d) Sequential R/W Test - Destructive.
e) Disk Change Line Test- Non-destructive.

Diskette Format - (Destructive)

This test allows an user to check out the NEC 765 controller's abilities to format a diskette.

The user need not be bothered about the dirve or the diskette in the drive. SYSTEM automatically determines the best way a diskette can be formatted for reliablity, e.g. In case of a 1.2MB drive the user need not specify whether the diskette to be formatted is 1.2 MB or 360 KB capacity. SYSTEM finds the most reliable format automatically.

Note that this test does not write a DOS format on the diskette.

Drive Speed Test - (Non-Destructive)

The test determines the speed of rotation of the drive. Please note that the following are the allowable speeds for the various drives:

a) 1.2 MB drive - 360 rpm for a 1.2 Mb diskette in it.
- 300 rpm for a 360Kb diskette in it.

b) 360 KB drive - 300 rpm.
c) 720 KBB drive - 300 rpm.

Allow for a tolerance of 1% on all the speeds.
Ensure that the diskette is formatted before performing this test.

Random Read/Write Test - (Destructive)

This test performs a random read/write operation on the diskette & thus checks out the random seek capability of the drive.

Again ensure that the diskette is formatted before perfor ing this test.

J1 (Select EPROM Size)

Set the jumper according to the type of chips used for the ROM BIOS:

1-2	Short	27256 chips
2-3	short	27128 chips

J19 (DRAM Access Timing)

Set this jumper according to the right DRAM access timing.

1-2	short	80/100 ns
2-3	short	120/150 ns

J28 (Select Backup Battery)

1-2	short	Onboard battery
2-3	short	Backup battery

J30 (Select FASTMODE or NORMAL)

FASTMODE requires zero wait state operation at 12MHz.

1-2	**short**	**FASTMODE**
2-3	**short**	**NORMAL**

J31 (Select One or Zero Wait State)

Do not change the wait stcte in cystem running.

ON	Zero wait state
OFF	One wait state

J102 (Select Oscillator)

The default oscillator on the 12MHz system board is a 48MHz oscillator (OSC1). The system provides a spare socket for another frequency oscillator (OSC2). If OSC2 is installed, you can run the system at the OSC2 clock rate.

1-2	short	Select OCS1
2-3	short	Select OCS2

Scan/ASCII Code Test

Upon invoking this test a keyboard layout is shown on the screen. This keyboard layout might not necessarily correspond with your keyboard.

The objective of this test is to determine whether the keys depressed match with their scan code.

Thus every time a key is depressed the scan code & the ASCII code of the key is shown.

Use <CNTRL> <BREAK> key to abort this test.

Function keys 11 & 12 in an Enhanced keyboard cannot be checked out by this test.

Video Diagnostics

Video diagnostics includes the following:

a) Sync Test - Checks the Sync capability.
b) Adapter Test - Performs test on the Display Memory.
c) Attribute Test - Checks the attributes of the Display memory
d) 80 x 25 Display Test - Checks the 80 x 25 character set of the display adapter.

The video diagnostics requires very little input & the results can be visually observed.

Miscellaneous Diagnostics

This includes the following tests:

a) Serial Communication Port Test.
b) Printer Port Test.

Serial Communication Port Test

This test requires a special RS-232C connector to be plugged on to the port.

The details of this connector are as below:

- RD & TD Shorted.
- DST & DTR Shorted.
- CTS & RTS Shorted.

This test exercises the port for different:

-Baud Rates

J1 (POWER Connector)

The pin assignments for the power connector J1 are as follows:

J1:

Pin	Assignment	Color
1	Power Good	Orange
2	+5v	Red
3	+12V	Yellow
4	-12V	Blue
5	GND	Black
6	GND	Black

J1:

Pin	Assignment	Color
1	GND	black
2	GND	black
3	-5V	white
4	+5V	red
5	+5V	red
6	+5V	red

J2 (Keyboard Connector)

The keyboard connector is a 5-pin, 90-degree PCB mounting, DIN connector. The pin assignments are as follows:

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	NC
4	GND
5	+5V

J3 (External Battery Connector)

The pin assignments are as follows:

Pin	Assignment
1	V+
2	NC
3	GND
4	GND

J19 and J20 (Hardware Speed and Hardware Reset Switch)

J19 is the hardware speed switch. This switch is a button switch or post jumper for selecting the system operation at high or low speed. This switch only works if JP9 is short.

J20 is the hardware reset switch. It is used for the hardware reset button.

J21 (Speaker Connector)

The pin assignments are as follows:

Pin	Assignment
1	SPEAK OUT
2	NC
3	GND
4	+5V

J22 (Keylock/Power LED)

The keylock and power LED is a 5-pin berg strip. Its pin assignments are as follows:

Pin	Assignment
1	GND
2	Keyboard inhibit
3	GND
4	not used
5	Power LED

J10 (Turbo Indicator Connector)

The system speed LED indicator indicates the current operating speed of the system. When the LED lights up, the system is operating at high speed.

The pin assignments are

Pin	Assignment
-	GND
+	plus driver

J4 (Select Backup Battery)

2-3	short	Onboard battery
1-2	short	Backup battery

JP1 (Select FASTMODE or NORMAL)

FASTMODE requires zero wait state operation at 12MHz.

short	FASTMODE
open	NORMAL

J12 (Select Oscillator)

The default oscillator on the 12MHz system board is a 48MHz oscillator (OSC1). The system provides a spare socket for another frequency oscillator (OSC2). If OSC2 is installed, you can run the system at the OSC2 clock rate.

1-2	short	Select OCS1
2-3	short	Select OCS2

J3 (Select One or Zero Wait State)

Do not change the wait stcte in cystem running.

ON	Zero wait state
OFF	One wait state

JP5 (DRAM Access Timing)

Set this jumper according to the right DRAM access timing.

1-2	short	80/100 ns
2-3	short	120/150 ns

JP6 (Select EPROM Size)

Set the jumper according to the type of chips used for the ROM BIOS:

1-2	Short	27128 chips
2-3	short	27256 chips

JP7,8,9 (Speed Control Mode)

These three jumpers are used to control the speed mode One of the three jumpers should be short.

JP7	short	Keyboard switch, signal from P13 (pin 30) of 8042
JP8	short	Keyboard switch, signal from P22 (pin 23) of 8042
JP9	short	for hardware speed switch

SW1,2,3 (Select RAM Size)

The system allows 5 onboard memory options for supporting up to a full 4MB system. The memory mapping options are shown in Table 6.

Table 6 RAM Configuration

Bank 0	18X256K	18X256K	18X256k	18X1M	18X1M
Bank 1		18X64K	18X256K		18x1M
SW-1	ON	OFF	ON	OFF	ON
SW-2	ON	ON	OFF	OFF	ON
SW-3	ON	ON	ON	ON	OFF

NOTES: Bank 0 comprise of the 18 sockets on top labeled from U1 to U18 or the slots (SIP) labeled slot1 and slot3.

Bank 1 comprise of the 18 sockets on the bottom labeled from U19 to U36 or the slots (SIP) labled slot2 and slot4.

SW4 (Enable Color)

ON	Color
OFF	Monochrome

USING SETUP

Before turning on the power to your system, check that all connectors are connected properly. Also check that all switches and jumpers are set correctly for your system configuration. To check how your system is configured, call out the SETUP routine. Refer to the BIOS menu for details.

I/O CHANNEL DEFINITIONS

The figures below shows the location and numbering of the I/O channel connectors which consists of eight 62-pin and six 36-pin card-edge.

Cards which IBM declares to be incompatible with the AT architecture and thus the AT baby board includes:

8-bit cards (62-pin connector only) containing system memory.

Cards which will work in the mainboard expansion bus includes:

AT compatible cards.
PC floppy disk controller card.
Some XT type hard disk controllers (including Xebec, Western Digital, and CDC). Refer to the technical reference manual for the details on installation.
Most 8-bit display adapters.
Most 8-bit cards containing I/O functions only.
DTC 5290 or equivalent Hard 3 Floppy Disk Controller Floppy.

Table 7 I/O Address Map

Address (Hex)	Device
0-1F	DMA Controller #1 (82C37) - 8-bit devices
20-3F	Programmable Interrupt Controller #1 (82C59A)
40-5F	Timer/Controller (82C54)
60,64	Keyboard controller (8742)
61	On-board Testing Registers
70,71	Clock/Calendar (146818)
70,bit 7	NMI Mask
78	On-board Test Stimulus Register
80-9F	DMA Page Register
80	Diagnostic Port Location
A0-BF	Programmable Interrupt Controller #2 (82C59A)
C0-DF	DMA Controller #2 (82C37A) 16-bit Devices
F8-FF	Math Coprocessor

Figure 3 36-Pin Card-Edge Connector

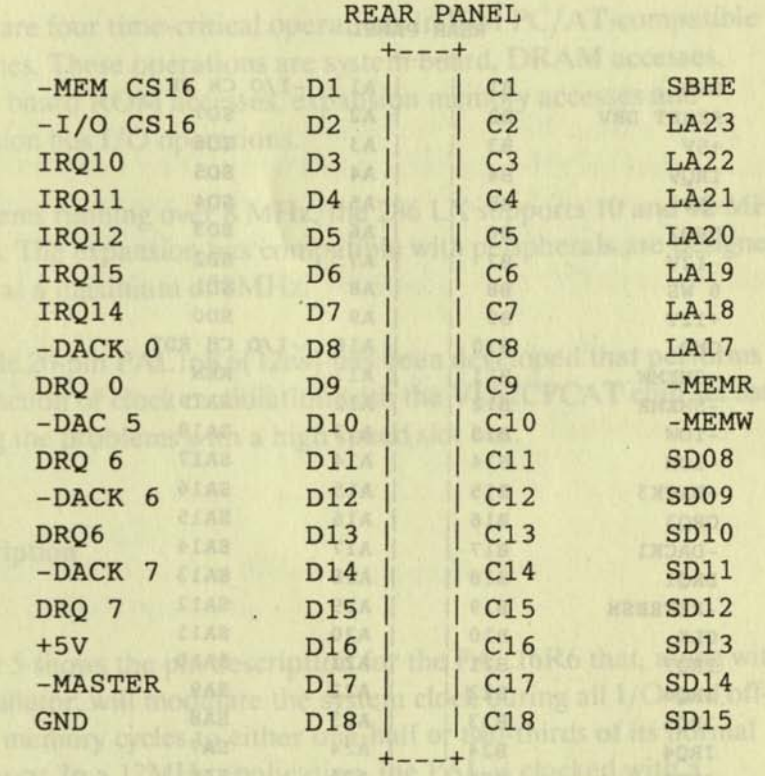
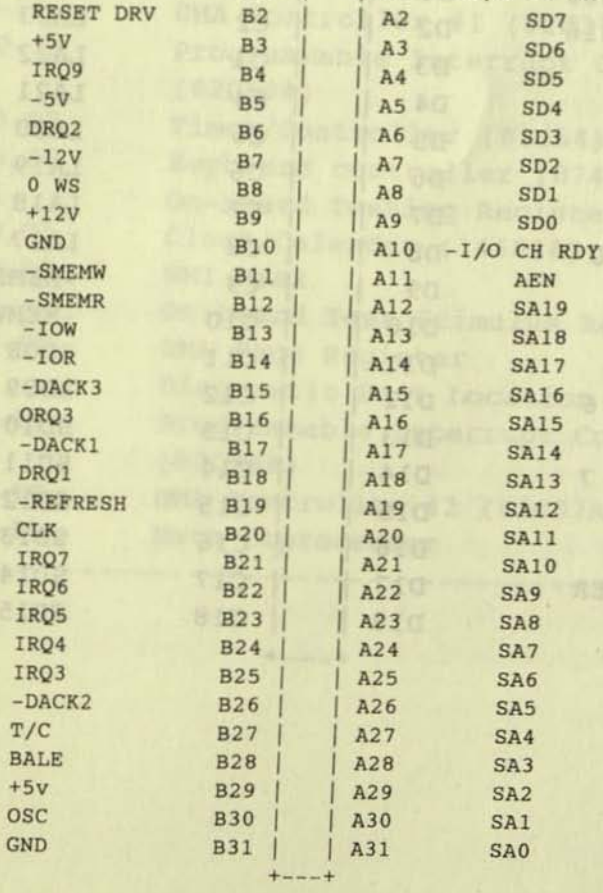


Figure 4 62-Pin Card-Edge Connector



System Clock Modulation

There are four time-critical operations in IBM PC/AT-compatible machines. These operations are system board, DRAM accesses, system board ROM accesses, expansion memory accesses and expansion bus I/O operations.

In systems running over 8 MHz, the 286 LX supports 10 and 12 MHz speeds. The expansion bus compatible with peripherals are designed to run at a maximum of 8MHz.

A single 20-pin PAL16R6(12ns) has been developed that performs the function of clock modulation with the VL82CPCAT chip set for solving the problems with a high speed slot bus.

PAL Description

Figure 5 shows the pin description for the PAL16R6 that, along with an oscillator, will modulate the system clock during all I/O and off-board memory cycles to either one-half or two-thirds of its normal frequency. In a 12MHz application, the PAL is clocked with a 48MHz oscillator and normally generates a 24-MHz clock which is used to drive the XTAL2(2) input (pin 84) of the VL82C101 (XTAL2(1) is left unconnected). The PAL samples the CPU status lines (S0, S1 and M/IO) and the F16 output of the VL82C102 just prior to the second phase 1 of PROCCLK in the status cycle (when

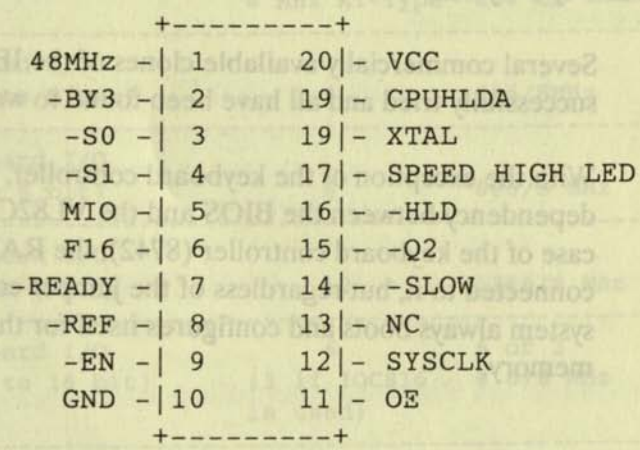
ALE is due to come out). If an I/O or off-board memory cycle is detected, the PAL outputs either 16MHz or 12Mhz clocks until the end of the cycle.

Table 8 shows the effect of clock modulation down to 6 or 8MHz in a 12MHz system. Because the decision as to the speed of the cycle is made before ALE is generated, it can be seen that many problem areas are covered. It should be noted here that clock modulation only lengthens the ALE pulse width in the case that the operation is detected as an I/O cycle or an off-board memory cycle.

The clock modulation PAL appears to provide an effective way to make a 12 MHz AT-compatible system that is truly compatible on the expansion bus.

Figure 5 Pin Description for Clock Modulation PAL

PAL16R6(Note)



NOTE: Must be a 12ns PAL or equivalent for 12 MHz operation.

Other Considerations

Basic I/O System

Several commercially available clones of the IBM BIOS have been successfully tried and all have been found to work properly.

With the exception of the keyboard controller, there is no hardware dependency between the BIOS and the VL82CPCAT chip set. In the case of the keyboard controller (8742), the RAMSEL0 line is connected to it, but regardless of the jumper configuration, the system always boots and configures itself for the actual available memory.

Table 8 Duration of I/O and Memory Cycles for Various System Configurations (Note)

	8 MHz AT-Type	286 LX
On-board I/O (8 to 8 bit)	6	6@6/8MHz
Off-board I/O (8 to 8 bit)	6	6@6/8 MHz
Off-board I/O (16 to 8 bit)	12	12@6/* Mhz
Off-board I/O (16 to 16 bit)	6 (3 if IOCS16 is used)	6 or 3 @ 6/8 MHz
On-board DRAM	3	3 (2 if 0 wait states)
On-board ROM	3	3 (4 if 2 wait states)
Off-board Memory (8 bit)	6	6@6/8 MHz
Off-board Memory (16 bit)	6 (3 if MEMCS16 is used)	6 or 3 @6/8MHz

Note: All values in System Clocks are at the maximum system frequency, unless otherwise noted.

TECHNICAL INFORMATION

Features of the VL82C100/82C101/82C102/82C103/82C104 PC/AT compatible Chip set

- Fully compatible with IBM PC/AT-type designs
- High-integration five-chip set
- Reduces non-memory system device count from 110 to 16
- Supports 12 MHz processor clock
- Devices are available as "cores" for user-specific designs
- All devices designed in CMOS for low power consumption

82C100 PC-AT Peripheral Controller

The VL82C100 PC/AT Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74LS573 octal three-state latches, a 74LS138 3-to-8 Decoder, and five other less-complex integrated circuits. Using this internal functionality, the VL82C100 interfaces the keyboard controllers as well as the real-time clock to the PC/AT system.

The device also supplies control signals to the I/O slots, the VL82C101 System Controller as well as the system ROMs.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C100 is individually available, or may be purchased as part of the complete five-device VL82C(PA/AT) kit.

82C101 PC/AT System Controller

The VL82C101 PC/AT system Controller replaces an 82C284 clock controller and 82C288 Bus Controller (both are used in 286-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately ten other less-complex integrated circuits used as Wait State logic. When used in 12 MHz systems utilizing 80ns DRAMs, the device provides the required one wait state for a "write" operation. a 12MHz system using 120ns DRAMs will be provided.

with one wait state for "write" and one wait state for a "read". The device accepts both the 24MHz crystal to control the system clock as well as the 14.318MHz crystal to control the microprocessor clock. It also supplies reset and clock signals to the I/O slots.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 4-pin plastic leaded chip carrier (PLCC) package. The VL82C101 is individually available, or may be purchased as part of the complete five-device IBM-PC/AT kit.

82C102 PC/AT Memory Controller

The VL82C102 PC/AT Memory Controller generates the row address strobe (RAS) and column address strobe (CAS) necessary to support the dynamic RAMs used in the PC/AT. In addition, the device allows four motherboard memory options for the user, up to a full 2M-byte system. Three of the four options allow a full 640K-bytes user area to support the disk operating system (DOS). In addition, the VL82C102 provides the upper addresses to the I/O slots, the chip select for the ROM and RAM memory, and drives the system's speaker.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C102 is individually available, or may be purchased as part of the complete five-device VL82C(PC/AT) kit.

82C103 PC/AT Address Buffer

The VL82C103 PC/AT Address Buffer provides the system with a 16-bit address bus input and 41 buffered drivers. The buffered drivers consist of 17 bidirectional system bus drivers each capable of sinking 20mA (50 'LS loads) of current and 200 picofarads of capacitance on the backplane; 16 bidirectional local bus drivers, each capable of sinking 8mA (20 'LS loads) of current; and eight memory bus drivers, also capable of sinking 8mA of current on-chip refresh circuitry supports both 256K-bit and 1M bit DRAMs. The VL82C103 provides addressing for the I/O slots as well as the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C103 is individually available, or may be purchased as part of the complete five-device VL82(PC/AT) kit.

82C104 PC/AT Data Buffer

The VL82C104 PC/AT Data Buffer provides 16-bit data bus input as well as 40 buffered drivers. The buffered drivers consists of 16 bidirectional system data bus drivers, each capable of sinking 20mA (50 'LS loads) of current; eight bidirectional local bus drivers, each capable of sinking 8Ma (20 'LS loads) of current. The VL82C104 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C104 is individually available, or may be purchased as part of the complete five-device VL82(PC/AT) kit.

RECOMMENDED REFERENCES

Hardware

Information is available for each of the devices included in the AT baby board from Intel and other semiconductor companies. Sources are shown below:

Intel:

1985 Component Data Book
80286 Data Sheet
iAPX 286 Hardware Reference Manual

IBM:

Guide to Operations - Personal Computer AT Installation
Setup Personal Computer AT Technical Reference Manual

Software

Intel:

iAPX 286 Programmer's Reference Manual
iAPX 286 Operating System Writer's Guide

IBM:

PC-DOS 3.1 Reference Manual

CMOS Clock/RAM

The internal clock circuitry uses 14 bytes of the 64-byte CMOS RAM, and the rest are used for configuration information. The CMOS RAM addresses are:

Table 9 CMOS RAM Addresses

Address	Description
00-0D	Real-time clock information
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drives A and B type
11	Reserved
12	Hard Disk type-drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte checksum
30	0 Low expansion memory byte
31	0 High expansion memory byte
32	0 Data century byte
33	0 Information flags (set during power on)
34-3F	Reserved by IBM

HARDWARE COMPATIBILITY

This chapter shows the difference between the AT compatible computers, such as the AT baby board, and the rest of the IBM Personal Computer family. It also contains information on what expansion cards will be compatible with the AT baby board or any AT class machine.

The following are hardware features of the IBM Personal Computer AT and the AT baby board that are not supported by the rest of the IBM Personal Computer family:

1. The AT baby board uses an Intel 80286 microprocessor. Programming considerations due to faster processing capability of the 80286 require programs to be written without loops or routines which are dependent on execution speed by the CPU. This is usually no problem, since this is just good programming practice.

2. The expansion slots have a 36-pin connector in addition to the 62-pin connector. Adapters designed to make use of the 36-pin connector are not compatible with other machines with only the 62-pin connector.

3. The I/O channel is different.

   a. The system clock signal should only be used for synchronization and not for applications requiring a fixed frequency.

   b. The 14.31818 MHz oscillator is not synchronous with the system clock.

   c. "ALE" is active during DMA cycles.

   d. The I/O write signal is not active during refresh cycles.

Figure 6 Block Diagram of the 286 LX-A

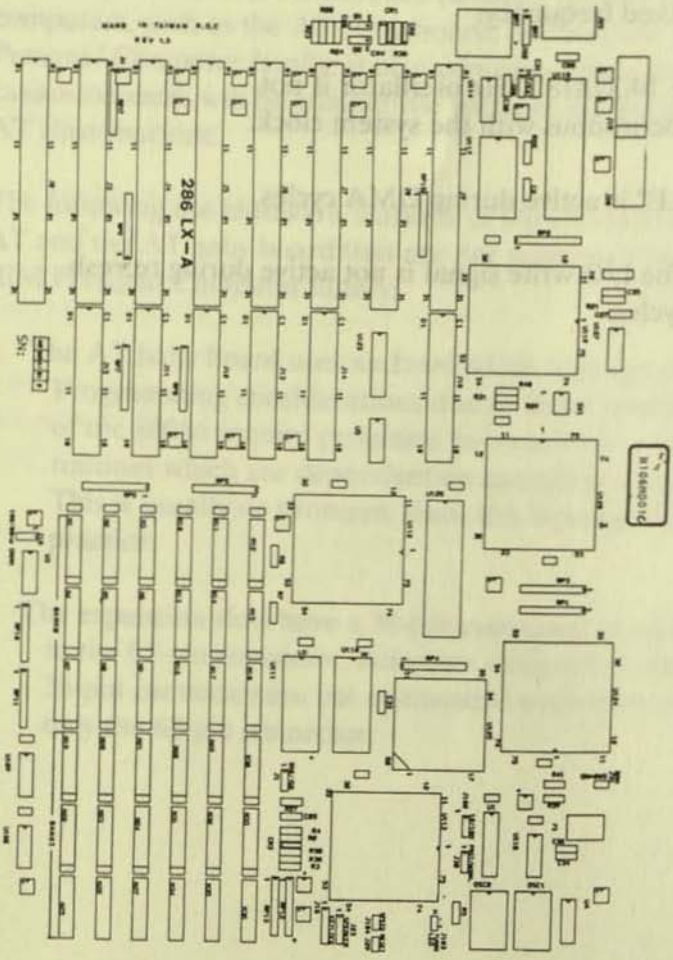
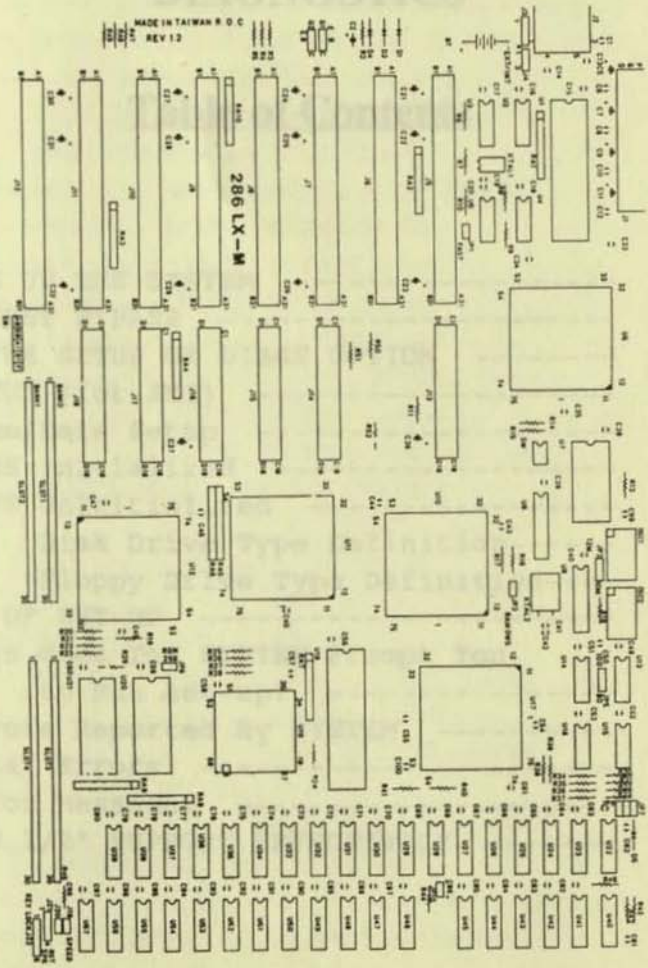
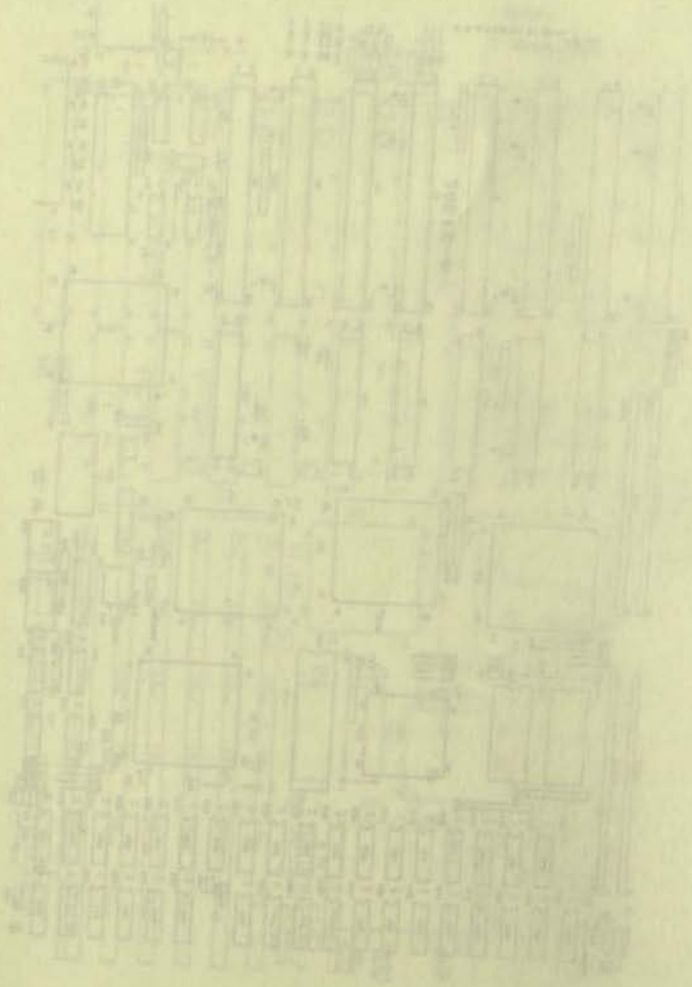


Figure 7 Block Diagram of the 286 LX-M



Notes:



CMOS SETUP AND DIAGNOSTICS

Table of Contents

SELECT THE SETUP OR DIAGS OPTION

Immediately after the memory and cache test, you will get the following prompt on the screen:

Press<DEL> key to run SETUP or DIAGS

Hit <DEL> key to get into the Setup Mode. Note that <DEL> key will get you into the set-up mode only when the message: Press <DEL> key to run SETUP or DIAGS, is displayed on the screen.

If you hit <DEL> key to the following message appears on the screen:

WANT TO RUN SETUP OR DIAGS (Y/N)?

If you answer <Y> or <y> followed by <ENTER> then you would be asked to select either Setup or Diagnostics as shown below:

SETUP or DIAG (1/2)?

Hit <1> to use the built-in SETUP option

Hit <2> to use the Advanced Diagnostics option.

CMOS SETUP (for AMI)

Time/Date Setup

The Setup screen looks like below:

C M O S S E T U P
Curret date is : XX-XX-XXXX
Enter new date (MM-DD-YYYY)?

To this question you would have to enter the date in the format shown on the screen.

If you feel that the current date should remain unchanged, you would just have to hit the <ENTER> key. In such a case the new date is set to the same value as the current date.

The next question you have on the screen is:

Current time is: XX:XX:XX
Enter new time (HH:MM:SS)?

To this question you key in the time in the format defined Press <ENTER> key alone if the current time is right.

As soon as you have done this the systme shows you the type of the display on your system.

PROCCLK

This is a 2X clock provided to the processor. In a 12Mhz system, this will be a 24MHz clock.

SYSCLK

This is the clock that corresponds to the actual 80286 execution. In a 12MHz system, this will be 12MHz.

FASTMODE

This mode allows for certain timing signals (RAMALE and RAS) to be generated earlier in a memory cycle than would have been by IBM-compatible logic. This option is required to allow no-wait state operation at 12 MHz.

RAMALE

This signal is an output of the VL82C101 that is used to allow CPU addresses to reach DRAMs earlier when FASTMODE is active. If FASTMODE is inactive, RAMALE behaves exactly like ALE in the IBM design. If FASTMODE is active, RAMALE will stay high, causing the memory address latches to be transparent whenever a memory read or write command is not taking place. If either command becomes active, RAMALE goes low latching the current address that is on the CPU address lines. This function of RAMALE makes memory addresses valid as soon as they propagate from the CPU

through the open latches instead of having to wait for ALE to go high.

RAS

When FASTMODE is inactive, this signal behaves as in the IBM design. When FASTMODE is enabled, RAS will go high one PROCCLK cycle before a memory read command.

ENDRAS

This is an output of the VL82C101 that allows sufficient RAS pre-charge time for the DRAMs between fast memory accesses. ENDRAS will normally go low three PROCCLK cycles after RAS goes high. ENDRAS will not return high until a minimum of 3ns after RAS returns low to avoid a spike on MEMRAS. Using fast memory timing with zero wait state DRAM accesses selected, ENDRAS will go low two PROCCLK cycles after RAS goes high.

MEMRAS

This signal is the logical NAND of RAS and ENDRAS. It is performed in logic that is external to the 82C100 chip set, and directly drives the RAS inputs of the memory array.

Your would then be asked to enter the type of the disk Drive D. The procedure for doing this is the same as that for Drive C. Remember if you do not have disk Drive D on your system. you just have to hit the <ENTER> key.

Floppy Drive Type Definition

Diskette drive A is 3 1/2" (Y/N)?

The above question is asked if the drive has been found to have 80 tracks. Since a drive with 80 tracks could either be a

- high capacity i.e. 1.2 MB drive
- or 3 1/2" i.e. 720 KB drive,

you would have to answer this question.
By entering <N> or <n> you can select the high capacity drive.

Alternatively enter <Y> or <y> to select a 720 KB drive. This question could come up for the case of drive B as well provided it has been detected as a 80 track drive by the System.

If you hit the <ENTER> key alone, the SYSTEM assumes the drive to be a 1.2 MB drive.

At this point you have entered all the information the SYSTEM requires for starting up the system.

At this point you have entered all the information the SYSTEM requires for starting up the system.

SYSTEM detects a few details by itself, e.g. the diskeete drive type in case of a 360KB drive as shown below:

Diskette drive B is : Double Sided (Other option as above)
Base Memory Size is.: XXX KB
Expansion memory size is :XXXX KB

Are these options correct (Y/N)?

If you are convinced at this stage that all the information you have entered upto this point is right, hit <Y> or <y> key followed by <ENTER> key. When you do this the SYSTEM goes all over again to boot up the system with the information specified.

However, if you would like to modify some information, then you should hit either <N> or <n> key followed by Enter. You would now go through the setup all over again.

The Main Board Components for 286 LX-A and 286 LX-M Systems

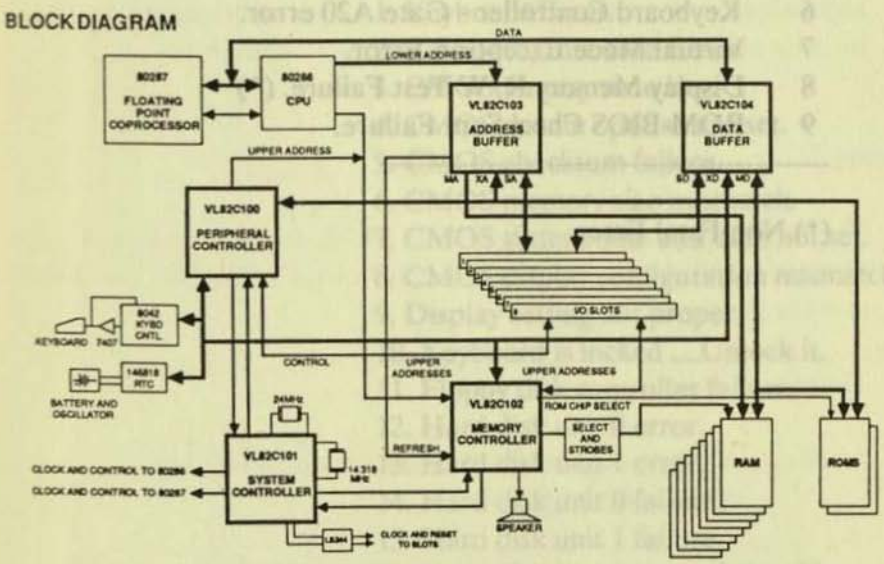
- AMD 80286 microprocessor
- 80287 math coprocessor socket
- Onboard memory socket for up to 4MB in 256K/1M step
- 128K/256K ROM selection
- Real-time clock with built-in rechargeable battery
- 8 expansion slots (6 dual 62/36-pin card-edge connectors and 2 62-pin card-edge connectors)
- 4-pin oscillator socket is provided for the optional 20MHz system clock

General Description

Block Diagram

The block diagram of the 286 LX baby board is shown in Figure 1.

Figure 1 Block Diagram of the 286 LX Baby Board



Fatal Errors

Beep Count	Meaning
1	DRAM refresh failure.
2	Parity Circuit failure.
3	Base 64KB RAM failure.
4	System Timer failure.
5	Processor Failure
6	Keyboard Controller - Gate A20 error.
7	Virtual Mode Exception Error.
8	Display Memory R/W Test Failure. (*)
9	ROM-BIOS CheckSum Failure.

(*) Non-Fatal Error.

Error Messages

Fatal Errors

1. Channel -2 of Timer Not functional.
2. Stray Interrupt sensed in controller.
3. Interrupt controller #2 not functional.

Non-Fatal Errors

1. Keyboard Error.
2. Keyboard/Interface Error.
3. CMOS battery state low.
4. CMOS system options not set.
5. CMOS checksum failure.
6. CMOS memory size mismatch.
7. CMOS system time and date not set.
8. CMOS display configuration mismatch.
9. Display setting not proper.
10. Keyboard is locked ....Unlock it.
11. Floppy disk controller failure.
12. Hard disk unit 0 error.
13. Hard disk unit 1 error.
14. Hard disk unit 0 failure.
15. Hard disk unit 1 failure.
16. Hard disk unit 1 is not defined in CMOS.
17. Cache Memory Bad - Do Not Enable Cache.

System Expansion Bus

The 286 LX provides drive for up to 8 XT compatible cards (6 of which can be AT compatible with the second connector). The bus is directly driven by the CMOS chips of the VL82CPCAT family, and can have to 50 LSTTL loads (DC drive capability = 20 mA) and 200pF. The 200pF is the practical limitation to systems since a conservative rule of thumb is that PC compatible cards rarely exceed 25 pF per pin. The 200 pF limitation allows for all 8 slots to be populated and not violate any of the drive specifications. For expansion bus 8-bit accesses, 4 wait states are automatically added in, thus making reads and writes into 6-cycle operations.

Timers

The VL82C100 chips contains an 82C54 timer which provides three programmable timers, each being driven with 1.19MHz. The timers provide for the following:

Timer	Usage
0	Directly drives IRQ to provide a periodic tick to the operating system.
1	Provides a refresh request to the DRAM control circuit. Normally set to a value of 12H, this timer generates a refresh request every 15us.
2	Provides the speaker output frequency.

Interrupt Controllers

The VL82C100 includes two 82C59A Programmable Interrupt Controllers that control interrupts to the 80286 CPU. When an interrupt line is driven as a result of the state of a signal on the expansion bus, Table 1 lists the signal and the type of source (8-bit or 16-bit). The 8-bit slots are the 62-pin connectors and the 16-bit slots are the 36-pin expansion slots. Table 1 shows the interrupt line usage.

f) Note that the Block Cursor is on the Hard Disk & the first option under hard disk diagnostics - Hard Disk Format.

Key Conventions

Use the Up & Down arrow keys to move within a Diagnostics Options Window.

Use the <ENTER> key to select the option in the Diagnostics Options Window.

Use <ESC> key to abort & return to previous menu.

Diagnostics Options Window

The individual diagnostics option window is as below:

a) Fig - 1 for Hard Disk Options.
b) fig - 2 for Floppy Disk Drive Options.
c) Fig - 3 for Keyboard Options.
d) Fig - 4 for Video Options.
e) Fig - 5 for Miscellaneous Options.

Hard Disk Diagnostics

Using Hard Disk Options

The Hard Disk options discussed below fall in -two categories:

a) Destructive Operation - The data on the Hard Disk is lost
b) Non-destructive Operation - The data on the Hard Disk is undisturbed.

The list below gives the various Hard Disk Options & the category they fall in:

a) Hard Disk Format -- Destructive Operation.
b) Auto Interleave -- Destructive Operation.
c) Media Analysis -- Destructive Operation.
d) Performance Test -- Non-destructive Operation.
e) Seek Test -- Non-destructive Operation.
f) Read/Verify Test -- Non-destructive Operation.
g) Check Test Cylinder --Data on the Test Cylinder alone is lost.

System Cycle Times

A summary of the system cycle times for various operations is shown in Table 3. The times to perform these operations are stated in both CPU cycles and actual time for a 12Mhz system. For DMA cycles, n equals the number of bytes or words that are being transferred. Thus, a DMA cycle to read one 16-bit word from off board will take 83.3* (22+8*(1-1))ns = 1883ns.

Table 3 System Cycle Times

Operation	CPU Cycles (12 MHz)	Time (ns)
16-bit Operations		
Read, 0 wait states(*1)	2	167
Read, 1 wait state (*1)	3	250
Write, 1 wait state (*1)	3	250
Read, 1 wait state (*1)	3	250
Write, 1 wait state (*1)	3	250
DMA read (*1)	22+8*(n-1)	83.3*(22+8*(n+1))
DMA write (*1)	22+8*(n-1)	83.3*(22+8*(n+1))
DMA read (*2)	22+8*(n-1)	83.3*(22+8*(n+1))
DMA write (*2)	22+8*(n-1)	83.3*(22+8*(n+1))
8-bit Operations		
DMA read (*1)	30+8*(n-1)	83.3*(30+8*(n+1))
DMA write (*1)	30+8*(n-1)	83.3*(30+8*(n+1))
DMA read (*2)	30+8*(n-1)	83.3*(30+8*(n+1))
DMA write (*2)	30+8*(n-1)	83.3(30+8*(n+1))
ROM Accesses		
Reads, 1 wait state	3	250
reads, 2 wait states	4	333
Refresh Cycles	5	417

Notes: *1 : on-board; *2 : off-board

Note that this USER definition is valid only as long as the Diagnostics is in effect. This feature is provided for you to test a disk drive, the definition for which is not available in the ROM.

b) Interleave Factor

Choose an optimum interleave factor. Refer to the Appendix - A for details on how to decide on an Optimum interleave.

The default value for the interleave factor is 3.

c) Mark Bad Tracks

If the manufacturer has defined certain bad patches on the disk, enter <Y> to this question.

The user then goes into a menu which allows for complete editing fo the bad track list.

Exit Bad track entry by hitting <ESC> or selecting the Save And Exit option. note the usage of <ESC> key here.

The default answer for this question is <N>.

d) Cylinder Number

Enter the Start & End Cylinder Number if you want to override the defaults.

The same is true for Start & End Head number.

The default value for the start Cylinder & Head is 0 and that of the End cylinder & head is the value of the maximum cylinder & head respectively.

e) Proceed

If all the entries are correct, you could hit <Y>. Else you could say <N> & go over all the entries again.

The default answer is <N>

f) Warning

If you had hit <Y> to the previous question, you get a WARNING message. You could preceed to format if you are absoultely sure about the information you have entered upto this point.

Table 4 Description of the Main Board Connectors, Jumpers and Switches

Location	Function
J18	Keylock/Power LED
J19	Power connector
J20	Power connector
J22	External battery connector
J23	Speaker connector
J25	Keyboard connector
J29	Hardware reset switch
J103	Indicator connector
J104	Hardware speed switch
J1	Select EPROM size
J10	DRAM access timing
J28	Select backup battery
J30	Select FASTMODE or NORMAL
J31	Select one or zero wait state
J102	Select oscillator
SW-1	Select RAM size
SW-2	Select RAM size
SW-3	Select RAM size
SW-4	Enable color

The following sections show the pin assignments for each connector or jumper.

J18 (Keylock/Power LED)

The keylock and power LED is a 5-pin berg strip. Its pin assignments are as follows:

Pin	Assignments
1	GND
2	Keyboard inhibit
3	GND
4	Not used
5	Power LED

Performance Test - (Non-Destructive Operation)

This test enables the user to check out his disk performance The critical factor in deciding the disk performance is the Interleave Factor. Changing the Interleave factor can bring about drastic changes in Disk Performance.

This test determines the Data Transfer Rate & the Track to Track Seek time. Data Transfer Rate is measured in the units Kilobytes/Second & the Track to Track seek time in milliseconds.

Higher value for Data transfer rate implies a better disk perfomance & lower value of track to track seek time indicates a better disk.

Refer to Appendix A for more on Interleave Factor & how to choose the same for best Disk Performance.

Seek Test - (Non-Destructive Operation)

This test checks the seek capability of the HardDisk on the specified Cylinder & Head range. First a sequential seek is performed & then a random seek is performed.

Any errors druing this test are reported.

Read/Verify Test - (Non-Destructive Operation)

This test performs sequential & random read & verify operation on the specified Cylinder, Head range.

Force Bad Tracks - (Destructive Operation)

This operation enables an User to define a set of tracks as bad. Certain specific applications require this option.

Floppy Diagnostics

All the options under floppy diagnostics require more or less the require the following inputs:

a) Drive No.
b) Start Track No.
d) End Track No.

J23 (Speaker Connector)

The pin assignments are as follows:

Pin	Assignment
1	SPEAK OUT
2	NC
3	GND
4	+5V

J25 (Keyboard Connector)

The pin assignments are as follows:

Pin	Assignment
1	Keyboard clock
2	keyboard data
3	NC
4	GND
5	+5V

J9 (Hardware Reset Switch)

This connector is used for the hardware reset button.

J103 (Turbo Indicator Connector)

The system speed LED indicator indicates the current operating speed of the system. When the LED lights up, the system is operating at high speed.

The pin assignments are

Pin	Assignment
-	GND
+	plus driver

J104 (Hardware Speed Switch)

This jumper is used to set the system speed. The system speed can be set to low or high speed. Short two pins for high speed.

Selecting the system speed through jumper setting is called hardware select and it has priority over the software select (through keyboard).

Sequential Read/Write Test - (Destructive)

This test performs a Sequential read/write operation & checks out the sequential seek, read & write capability of the dirve.

This test requires a formatted diskette.

Disk Change Line Test - (Non-Destructive)

This test is valid only for drives with the disk change line feature namely:

-1.2 Mb dirve
-720Kb or 3 1/2" drive.

This test checks whether the status of the disk change line changes when the diskette is removed /inserted in the drive.

This test requires a formatted diskette.

Keyboard Diagnostics

There are two types of diagnostics performed on the keyboard/keyboard controller.

They are:

a) Controller Test.
b) Sean/ASCII Code Test

Controller Test

This test exercises the keyboard controller & the keyboard status flags & takes about 2 minitues. Any error resulting from this test is reported.

Observe the CAPS, NUM & SCROLL LED's going on & off during the course of this test.

SW1,2,3 (Select RAM Size)

The system allows 5 onboard memory options for supporting up to a full 4MB system. The memory mapping options are shown in Table 5.

Table 5 RAM Configuration

Bank 0	18X256K	18X256K	18X256k	18X1M	18X1M
Bank 1		18X64K	18X256K		18x1M
SW-1	ON	OFF	ON	OFF	ON
SW-2	ON	ON	OFF	OFF	ON
SW-3	ON	ON	ON	ON	OFF

NOTES: Bank 0 comprise of the 18 sockets on top labeled from U1 to U18.

Bank 1 comprise of the 18 sockets on the bottom labeled from U19 to U36.

SW4 (Enable Color)

ON	Color
OFF	Monochrome

The Jumpers, Connectors and Switches in 286 LX-M

Location	Function
J1	POWER connector
J2	Keyboard connector
J3	External battery
J19	Hardware speed switch
J20	Hardware reset switch
J21	Speaker connector
J22	Keylock/Power LED
JP10	Turbo Indicator connector
J4	Select backup battery
JP1	Select FASTMODE or NORMAL
JP2	Select oscillator
JP3	Select one or zero wait state
JP5	DRAM access timing
JP6	Select EPROM size
JP7	Select speed control mode
JP8	Select speed control mode
JP9	Select speed control mode
SW-1	Select RAM size
SW-2	Select RAM size
SW-3	Select RAM size
SW-4	Enable color

-7 Bit/ 8 Bit &
-Odd / Even Parity

The results of the test are shown on the screen.

Printer Port Test

This test writes a pattern on the Printer & the results are observed on the Printer.

APPENDIX A

INTERLEAVE FACTOR - WHAT IS IT?

To understand the meaning of Interleave associated with Hard Disks, we shall take you thru' an analogy. We hope we have made the meaning clear when we finish the analogy.

Consider the game of a roulette where a round table is set in motion & people wait for the motion to stop on their lucky number.

We shall add a slight twist to this game.

Assume we have 17 sectors on the roulette round table & that we have 17 coins numbered & stacked up in the order 1 through 17 with coin 1 at the top.

We shall now set the round table in motion at a reasonable speed & give ouselves the task of placing the coin from the stack pile on every sector taking the minimum time and remaining static at one place during the course of the game.

Assume you have placed coin 1 in a certain sector. By the time you pick up the next coin & place it, the immediate sector following coin 1 would have passed you. So what you would then do, is to place it on the sector just passing by.

Thus after placing the coins in all the sectors, you should stop the roulette table & look at coins numbers in the contiguous sectors.

You are sure to find that they are not in an increasing order. You soon realise that this disorder is due to the fact that the game requires you to place all the coins in minimum time.

If you had wanted the coins in an order, you would have had to wait for at least 17 revolutions before placing all the coins.

The average number of contiguous sectors between a sector occpied by coin 'n' & by coin 'n+1' can be termed as Interleave factor.

In this analogy the Hard Disk is the roulette table in motion at a constant speed of 3600 rpm & the person can be visualised as the head & the related data transfer hardware.

Information is organised in sectors & the sectors are accesed by their numbers. Thus using a specific interleave to number the sectors helps in achieving a data transfer rate change.

For a Hard disk with factory specified access times, the only factor in the control of th user is the Interleave factor.

We realise this & we have the Auto Interleave feature which does exactly this.

Thus it is important that the value chosen gives the best performance.

APPENDIX B & FIGURES

HARD DISK TYPE

Type	Cylinders	Heads	Write-precomp	Landing-zone	capacity
1	306	4	128	305	10MB
2	615	4	300	615	21MB
3	615	6	300	615	31MB
4	940	8	512	940	64MB
5	940	6	512	940	48MB
6	615	4	NONE	615	21MB
7	462	8	256	511	31MB
8	733	5	NONE	733	31MB
9	900	15	NONE	901	115MB
10	820	3	NONE	820	21MB
11	855	5	NONE	855	36MB
12	855	7	NONE	855	51MB
13	306	8	128	319	21MB
14	733	7	NONE	733	44MB
15	000	0	000	000	00MB
16	612	4	ALL CYLS.	663	21MB
17	977	5	300	977	42MB
18	977	7	NONE	977	58MB
19	1024	7	512	1023	61MB
20	733	5	300	732	31MB
21	733	7	300	732	42MB
22	733	5	300	733	31MB
23	306	4	ALL CYLS.	336	10MB
24	925	7	ALL CYLS.	925	56MB
25	925	9	NONE	925	72MB
26	754	7	754	754	46MB
27	754	11	NONE	754	72MB
28	699	7	256	699	42MB
29	823	10	NONE	823	71MB
30	918	7	918	918	55MB

Type	Cylinders	Heads	Write-precomp	Landing-zone	capacity
31	1024	11	NONE	1024	98MB
32	1024	15	NONE	1024	133MB
33	1024	5	1024	1024	44MB
34	612	2	128	612	10MB
35	1024	9	NONE	1024	80MB
36	1024	8	512	1024	71MB
37	615	8	128	615	42MB
38	987	3	987	987	25MB
39	987	7	987	987	60MB
40	820	6	820	820	42MB
41	977	5	977	977	42MB
42	981	5	981	981	42MB
43	830	7	512	830	50MB
44	830	10	NONE	830	72MB
45	380	917	NONE	918	115MB
46	000	00	000	000	00MB

NOTE: **The Following figures are not same as shown from your AMI BIOS. However, the basic description is correct.**

Fig. 1

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk	Floppy	KeyBoard	Video	Miscellaneous

Hard Disk Format Auto Interleave
Media Analysis
Performance Test Seek Test Read/Verify Test Check Test Cyl.
Force Bad Tracks

Devices Present

Harddisk	Floppy	Commu.	Display	Printer	Memory	CO-proc
C:	A: 1.2MB	NONE	MONO	#03BC	REAL=512KB	ABSENT
					EXTD= 0KB	

Select - <ENTER> Exit Diag - <ESC>
Performat The Hard Disk

Fig. 2

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk	Floppy	KeyBoard	Video	Miscellaneous

Diskette Format
Drive Speed Test Ramdom R/W Test Sequential R/W Test
Disk Change Line Test

Devices Present

Harddisk	Floppy	Commu.	Display	Printer	Memory	CO-proc
C:	A: 1.2MB	NONE	MONO	#03BC	REAL=512KB	ABSENT
					EXTD= 0KB	

Select - <ENTER> Exit Diag - <ESC>
Format The Floppy Diskette

Fig. 3

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk	Floppy	KeyBoard	Video	Miscellaneous

Scan/ASCII Code Test

Devices Present

Harddisk	Floppy	Commu.	Display	Printer	Memory	CO-proc
C:	A: 1.2MB	NONE	MONO	#03BC	REAL=512KB	ABSENT
					EXTD= 0KB	

Select - <ENTER> Exit Diag - <ESC>
Check The Scan/ASCII Codes Of The Keyboard

Fig. 4

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk	Floppy	KeyBoard	Video	Miscellaneous

Run All Tests
Sync Test Adapter Test Attribute Test 80 x 25 Display Test

Devices Present

Harddisk	Floppy	Commu.	Display	Printer	Memory	CO-proc
C:	A: 1.2MB	NONE	MONO	#03BC	REAL=512KB	ABSENT
					EXTD= 0KB	

Select - <ENTER> Exit Diag - <ESC>
Perform All The Video Tests

Fig. 5

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk	Floppy	KeyBoard	Video	Miscellaneous

Printer Adapter Test
Commu. Adapter Test

Devices Present

Harddisk	Floppy	Commu.	Display	Printer	Memory	CO-proc
C:	A: 1.2MB	NONE	MONO	#03BC	REAL=512KB	ABSENT
					EXTD= 0KB	

Select - <ENTER> Exit Diag - <ESC>
Test Printer Controller

Fig. 6

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk Floppy KeyBoard

Hard Disk Format	
Disk Drive (C/D)	? C
Disk Drive Type	? 2
Interleave (1-16)	?
Mark Bad Tracks (Y/N)	?
Start Cylinder Number	?
End Cylinder Number	?
Start Head number	?
End Head number	?
Proceed (Y/N)	?

Type	Cyl.	Heads	W-pcomp	L-zone	Capacity
1	306	4	128	305	10MB
2	615	4	300	615	21MB
3	615	6	300	615	21MB
4	940	8	512	940	64MB
5	940	6	512	940	48MB
6	615	4	FFFF	615	21MB
7	462	8	256	511	31MB
8	733	5	FFFF	733	31MB
9	900	15	FFF	901	115MB
10	820	3	FFFF	820	21MB
11	855	5	FFFF	855	36MB
12	855	7	FFFF	855	51MB
13	306	8	128	319	21MB
14	733	7	FFFF	733	44MB
15	000	0	0000	000	00MB
16	612	4	0000	663	21MB

Device			
Harddisk	Floppy	Commu.	D
C:	A: 1.2MB	NONE	M

EXTD = 0KB

Select - <ENTER> Exit Diag - <ESC>
Preformat The Hard Disk

Fig-7

286-ROM DIAGNOSTICS, (C) 1986, American Megatrends Inc.

Hard Disk Floppy KeyBoard Video Miscellaneous

Hard Disk Format	
Disk Drive (C/D)	? C
Disk Drive Type	? 2
Interleave (1-16)	? 3
Mark Bad Tracks (Y/N)	? N
Start Cylinder Number	? 0
End Cylinder Number	? 614
Start Head number	? 0
End Head number	? 3
Proceed (Y/N)	? N

Bad Track List		
S#	Cyl.	Head
Entries # : 0		

Devices Present

Harddisk	Floppy	Commu.	Display	Printer	Memory	CO-proc
C:	A: 1.2MB	NONE	MONO	#03BC	REAL=512KB	ABSENT
					EXTD= 0KB	

Select - <ENTER> Exit Diag - <ESC>
Preformat The Hard Disk